I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 2002-45784 filed on August 2, 2002.

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[Abstract of the Disclosure]

[Abstract]

A magnetic random access memory (MRAM) is disclosed, in which current of (I(H)+I(L))/2 flows to a reference cell irrespective of a bitline clamp voltage. The MRAM includes a memory cell array block, a reference memory cell array block, a reference current providing unit, and a sense amplifier. Current of (I(H)+I(L))/2 regularly flows to a reference bitline irrespective of a bitline clamping voltage level, which make it possible to stably sense iT-i(H) or it-i(L) current of a bitline according to a selected memory cell value.

[Typical Figure]

FIG. 3

[Index]

MRAM, bitline clamp voltage, reference cell, magnetic memory cell

[Specification]

[Title of the Invention]

MAGNETIC RANDOM ACCESS MEMORY FOR FLOWING CONSTANT (I(H)+I(L))/2) CURRENT TO REFERENCE CELL WITHOUT REPARD OF BITLINE CLAMP VOLTAGE

[Brief Description of the Drawings]

FIG. 1 illustrates a conventional MRAM.

FIG. 2 illustrates a resistance value variation based on a bitline clamp voltage of FIG. 1.

FIG. 3 illustrates an MRAM according to an embodiment of the present invention.

FIG. 4 illustrates a reference current supply unit of FIG. 3.

FIG. 5 illustrates a bitline clamp circuit of FIG. 3.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a magnetic random access memory and, more particularly, to A magnetic random access memory (MRAM) in which current of (I(H)+I(L))/2 flows to a reference cell irrespective of a bitline clamp voltage.

A magnetic random access memory (hereinafter referred to as

"MRAM") is a kind of a nonvolatile memory device and includes a plurality of magnetic memory cells. An MRAM uses a magnetoresistive phenomenon occurring between a magnetic film and a non-magnetic film which are alternately stacked to constitute a multi-layer film. A magnetic resistance of a magnetic memory cell becomes maximum or minimum when magnetization directions are identical or opposite, respectively. The magnetization directions are identical, which is called a "parallel" state and indicates a logic "L" state. The magnetization directions are opposite, which is called a "non-parallel" state and indicates a logic "H" state.

In an MRAM, sense current and reference current are applied to a target cell and a reference cell so as to read a logic state stored in a magnetic memory cell, respectively. A voltage drop occurs at both ends of cells according to a magnetic resistance of the target cell and the reference cell. These voltages are compared with each other to determine a state of the target cell. To correctly compare the target cell with the reference cell, what is needed is a magnetic memory cell without variation of the magnetic resistance. It is general that current of (I(H)+I(L))/2 flows to a reference cell.

FIG. 1 shows FIG. 7 of an MRAM paper (VLSI symposium, 2002), which illustrates a 32Kb MRAM memory block embedding a mid-point reference generator. A mid-point reference generator has four magnetic resistors which are connected in series and parallel. A serially connected magnetic resistor is connected to another serially connected magnetic resistor, being a 1/2 (Rmax+Rmin) resistor. A magnetic resistance value of the mid-point reference generator may slightly vary with the level of a clamp voltage Vref, which will be described with reference to FIG. 2. Referring to FIG. 2, a difference between a maximum Rmax and a minimum Rmin when a bitline clamp voltage Vref is a set value is smaller than a difference between a maximum Rmax and a minimum Rmin when the reference voltage Vref is

smaller than a set value. That is, if the bitline clamp voltage Vref has a high level, a 1/2 (Rmax+Rmin) resistance value becomes small; if the bitline clamp voltage Vref has a low level, a 1/2 (Rmax+Rmin) resistance value becomes large. Accordingly, the mid-point reference generator must regulate a reference voltage Vref so as to adjust a 1/2 (Rmax+Rmin) resistor value, which is understood only by a test result. Moreover, a bitline clamp voltage of a reference cell should be reconfigured.

Therefore, what is needed is an MRAM in which current of (I(H)+I(L))/2 flows to a reference cell irrespective of a bitline clamp voltage.

[Technical Object of the Invention]

Therefore, it is an object of the invention to provide an MRAM in which current of (I(H)+I(L))/2 flows to a reference cell irrespective of a bitline clamp voltage.

In order to achieve the object, the present invention provides an MRAM comprising a memory array block having magnetic memory cells arranged in a matrix of rows and columns at intersections of wordlines, bitlines, and digit lines; a reference memory array block having a magnetic memory cell arranged in a matrix of rows and columns at intersection of the wordline, first and second reference bitline, and digit line; a reference current supply unit for supplying reference current to the reference bitline in response to a bitline clamp voltage; and a sense amplifier for comparing current flowing to the bitline and the reference current of the reference bitline according to the selected magnetic cell data in the memory cell array block to sense a data value of the selected magnetic memory cell.

Specifically, the reference current supply unit comprises a first current mirror connected to the first reference bitline and allowing a first bitline current to flow in response to the bitline clamp voltage; a second current mirror connected to the second reference bitline and allowing a

second bitline current to flow in response to the bitline clamp voltage; and a third current mirror for supplying half current of the sum of the first and second reference bitline current to the sense amplifier. The reference memory cell array block stores a logic high state in the magnetic memory cells connected to the first reference bitline and stores a logic low state in the magnetic memory cells connected to the second reference bitline. The MARAM further comprises a bitline clamp circuit for hold a data line through which the bitline current flows and a reference data line through which the reference bitline current flows with the use of the bitline clamp voltage when the wordline of the selected magnetic memory cell is enabled.

Therefore, according to an MRAM of the present invention, current of (I(H)+I(L))/2 flows to a reference data line irrespective of a bitline clamp voltage level to stably sense iT-I(H) or iT-I(L) current of a data line based on a value of a selected memory cell.

FIG. 3 illustrates an MRAM according to an embodiment of the present invention. An MRAM 300 includes a memory array block 310, a reference memory array block 320, a wordline selecting unit 330, a digit line selecting unit 340, a bitline/reference bitline selecting unit 350, a reference current supply unit 360, a bitline clamping circuit 370, and a sense amplifier 380. The memory array block 310 includes a magnetic cell arranged at intersections of wordlines WL0, WL1, WL2, and WL3 (totally called "WL"), bitlines BL0, BL1, BL2, and BL3 (totally called "BL"), and digit lines DL0, DL1, DL2, and DL3 (totally called "DL"). The reference memory array block 320 includes a magnetic memory cell arragned in an intersection of wordlines WL, reference bitlines RBL, and digit lines DL. Magnetic memory cells connected to a first reference bitline RBL0 store a logic "H" state, and magnetic memory cells connected to a second reference bitline RBL1 store a logic "L" state.

The wordline selecting unit 330 selects one of wordlnes WL, and the

bitline selecting unit 350 selects one of bitlines BL. The digit line selecting unit 340 selects one of digit lines DL and determines a direction of digit current ID.

The reference current supply unit 360 is shown more fully in FIG. 4 and includes first to third current mirrors 362, 364, and 366 connected to first and second reference bitlines RBL0 and RBL1 of the reference memory array block 320. The first current mirror 363 is connected to the first reference bitline RBL0 and allows i(H) current to flow to a first transistor 361 in response to a predetermined bitline clamp voltage VREF, allowing the i(H) current to a secon transistor 362. The first and second transistors 361 and 362 are identical in channel width and length. A second current mirror 363 is connected to the second reference bitline RBL1 and allows i(L) current to flow to a third transistor 364 in response to a predetermined bitline clamp voltage VREF, allowing the current i(L) current to a fourth transistor 365. The third and fourth transistors 364 and 365 are identical in channel width and length. The third current mirror 369 allows i(H)+i(L) current to a fifth transistor 367. The i(H)+i(L) current is a sum current of the i(H) and i(L) currents and is provided from the second and fourth transistors 362 and 365. A sixth transistor 368 is set to have half channel length of the fifth transistor 367, so that the current flowing to the sixth transistor 368 is (i(H)+i(L))/2.

The (i(H)+i(L))/2 current flowing to the reference current supply unit 360 flows to a reference data line through a reference bitline RBL. Bitline clamp current iT provided from the bitline clamp circuit 370 is added to the reference data line. Thus the (i(H)+i(L))/2 current flows to the reference data line, which is connected to a sense amplifier. The magnetic memory cell selected at the memory array block 310 is connected to a data line through a bitline. At this time, the current flowing to the bitline is the i(H) current or the i(L) current according to the logic state of the selected

memory cell. A bitline clamp current iT provided from the bitline clamp circuit 370 is added, so that iT-i(H) or iT-i(L) current flows to the data line.

The sense amplifier 380 senses and amplifies current flowing to a data line and a reference data line to determine a logic state of a selected magnetic meory cell. The current flowing to the reference data line is iT-(i(H)+i(L))/2 current, which should have a voltage level enough to turn on the first to fourth transistors 361, 362, 364, and 365 in the first and second current mirrors 363 and 366. This means that although the bitline clamp voltage VREF varies over a turn-on voltage of a transistor, currents flowing to a reference bitline and a reference data line are ((i(H)+i(L))/2 and iT-(i(H)+i(L))/2 which are constant, respectively.

Referring to FIG. 5, a bitline clamp circuit 370 is coupled between a data line, a reference data line, and a sense amplifier 380 and includes differential amplifier units 372 and 374, a driving unit 376, and a current supply unit 378. The differential amplifier units 372 and 374 feedbacks a data line voltage, controlling the driving unit 376 such that the data line voltage becomes identical to a bitline clamp voltage VREF. When a wordline is enabled, a data line precharged to a ground line and a reference data line go to a level of a bitline clamp voltage VREF and i(H) or i(L) current flows to the data line according to a data value of a selected memory cell.

Accordingly, current iT-(i(H)+i(L))/2 current constantly flows to the reference data line without regulating a level of the bitline clamp voltage VREF. In comparison with current iT-(i(H)+i(L))/2 current of the reference data line, an operation of a sense amplifier to sense current iT-i(H) or iT-i(L) current of a data line is stable.

While the present invention has been described with reference to specific embodiments thereof, it will be merely exemplary and various modifications and substitutes may be made without departing from the scope

and spirit of the invention.

[Effect of the Invention]

According to the foregoing MRAM of the present invention, (I(H)+I(L))/2 current flows to a reference data line irrespective of a level of a bitline clamp voltage to stably sense current iT-(i(H) or iT-i(L)) current based on a value of a selected memory cell.

[Scope of the Claim]

[Claim 1]

A memory device comprising:

a memory array block having magnetic memory cells arranged in a matrix of rows and columns at intersections of wordlines, bitlines, and digit lines;

a reference memory array block having a magnetic memory cell arranged in a matrix of rows and columns at intersection of the wordline, first and second reference bitline, and digit line;

a reference current supply unit for supplying reference current to the reference bitline in response to a bitline clamp voltage; and

a sense amplifier for comparing current flowing to the bitline and the reference current of the reference bitline according to the selected magnetic cell data in the memory cell array block to sense a data value of the selected magnetic memory cell.

[Claim 2]

The memory device of Claim 1, wherein the reference current supply unit comprises:

a first current mirror connected to the first reference bitline and allowing a first bitline current to flow in response to the bitline clamp voltage;

a second current mirror connected to the second reference bitline and allowing a second bitline current to flow in response to the bitline clamp voltage; and

a third current mirror for supplying half current of the sum of the

first and second reference bitline current to the sense amplifier.

[Claim 3]

The memory device of Claim 1, wherein the reference memory cell array block stores a logic high state in the magnetic memory cells connected to the first reference bitline and stores a logic low state in the magnetic memory cells connected to the second reference bitline.

[Claim 4]

The memory device of Claim 1, further comprising a bitline clamp circuit for hold a data line through which the bitline current flows and a reference data line through which the reference bitline current flows with the use of the bitline clamp voltage when the wordline of the selected magnetic memory cell is enabled.

Fig. 1

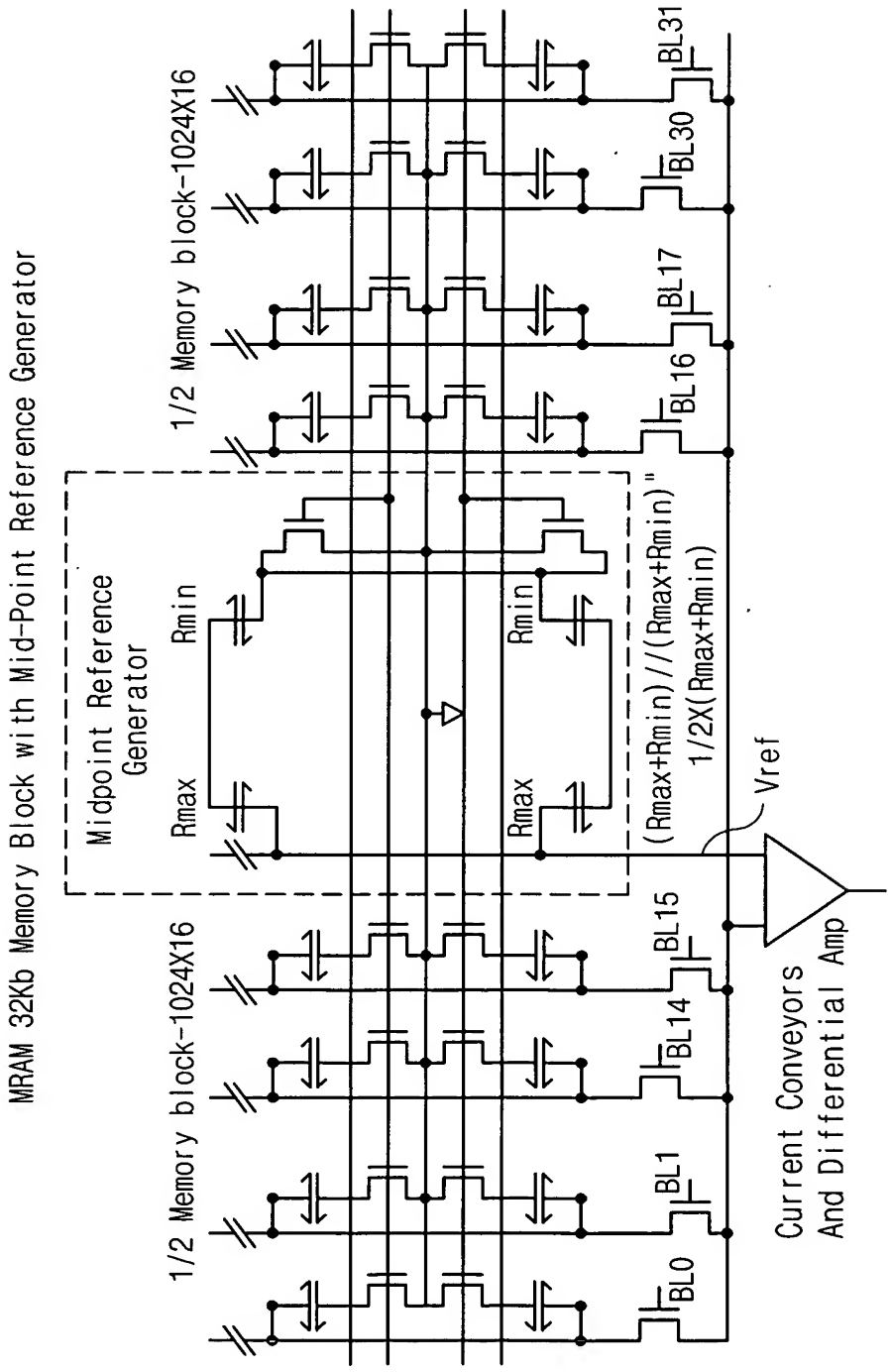


Fig. 2

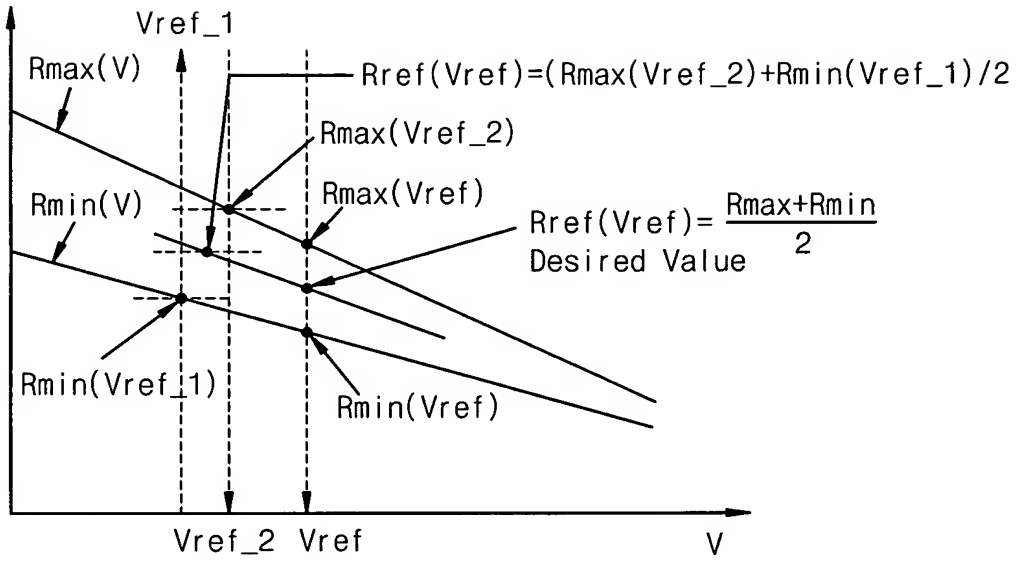

Vref_1
Rmax(V)
Rref(Vref)=(Rmax(Vref_2)+Rmin(Vref_1)/2
Rmax(Vref_2)
Rmax(Vref)
Rmin(V)
Rref(Vref)= Rmax+Rmin / 2
Desired Value
Rmin(Vref_1)
Rmin(Vref)
Vref_2
Vref
V

Fig. 3

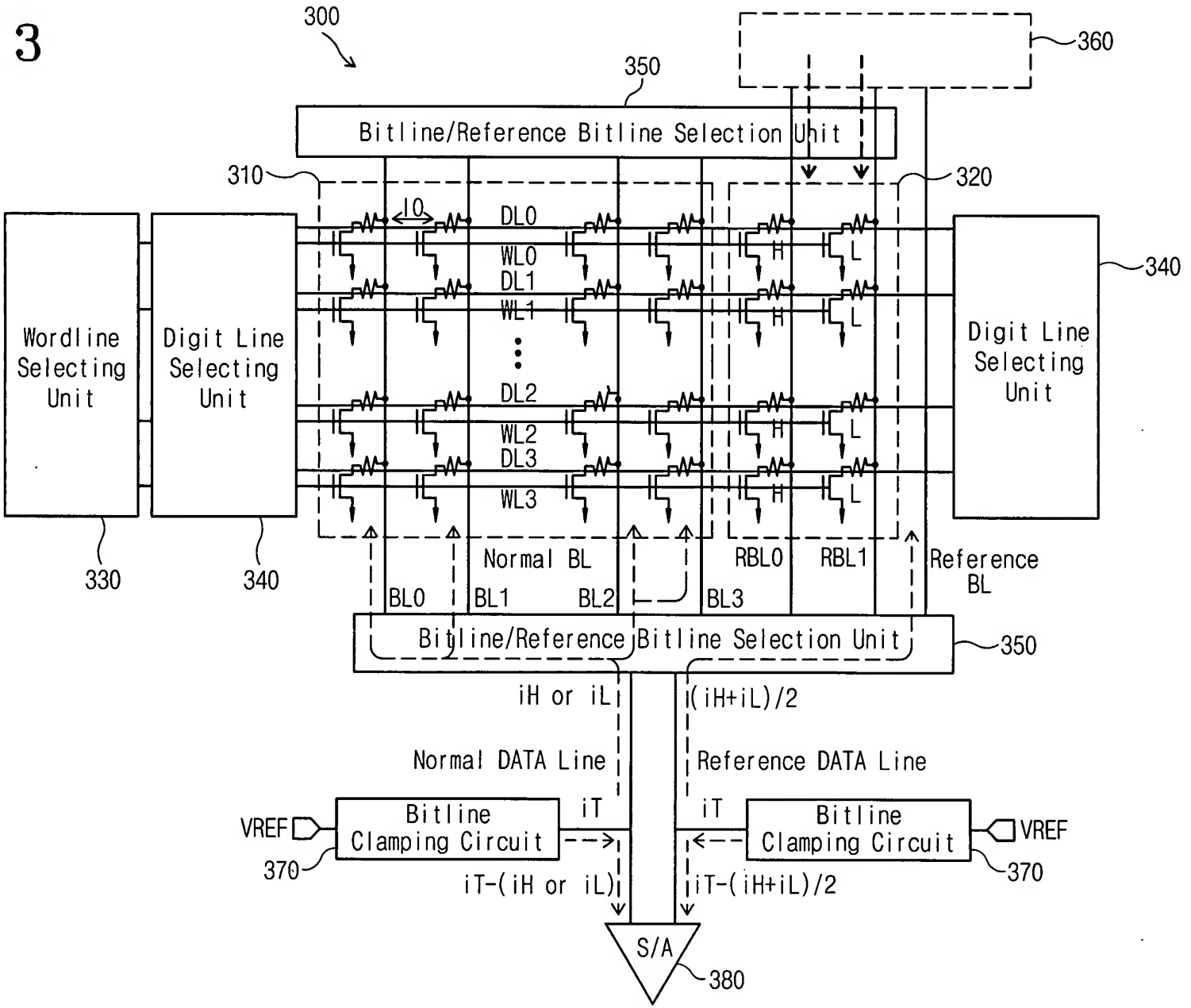
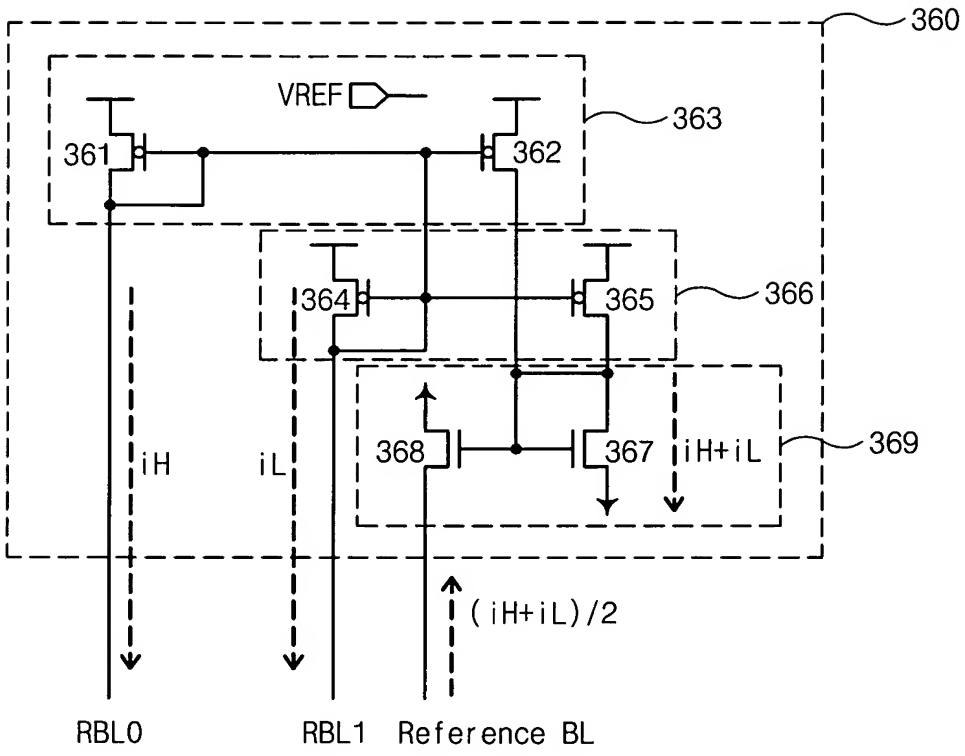

300
360
350
Bitline/Reference Bitline Selection Unit
310
320
10
DL0
WL0
DL1
WL1
DL2
WL2
DL3
WL3
H
L
Wordline Selecting Unit
Digit Line Selecting Unit
340
Digit Line Selecting Unit
330
340
Normal BL
RBL0
RBL1
Reference BL
BL0
BL1
BL2
BL3
Bitline/Reference Bitline Selection Unit
350
iH or iL
(iH+iL)/2
Normal DATA Line
Reference DATA Line
VREF
Bitline Clamping Circuit
iT
iT
Bitline Clamping Circuit
VREF
370
370
iT-(iH or iL)
iT-(iH+iL)/2
S/A
380

Fig. 4


360
VREF
363
361
362
364
365
366
368
367
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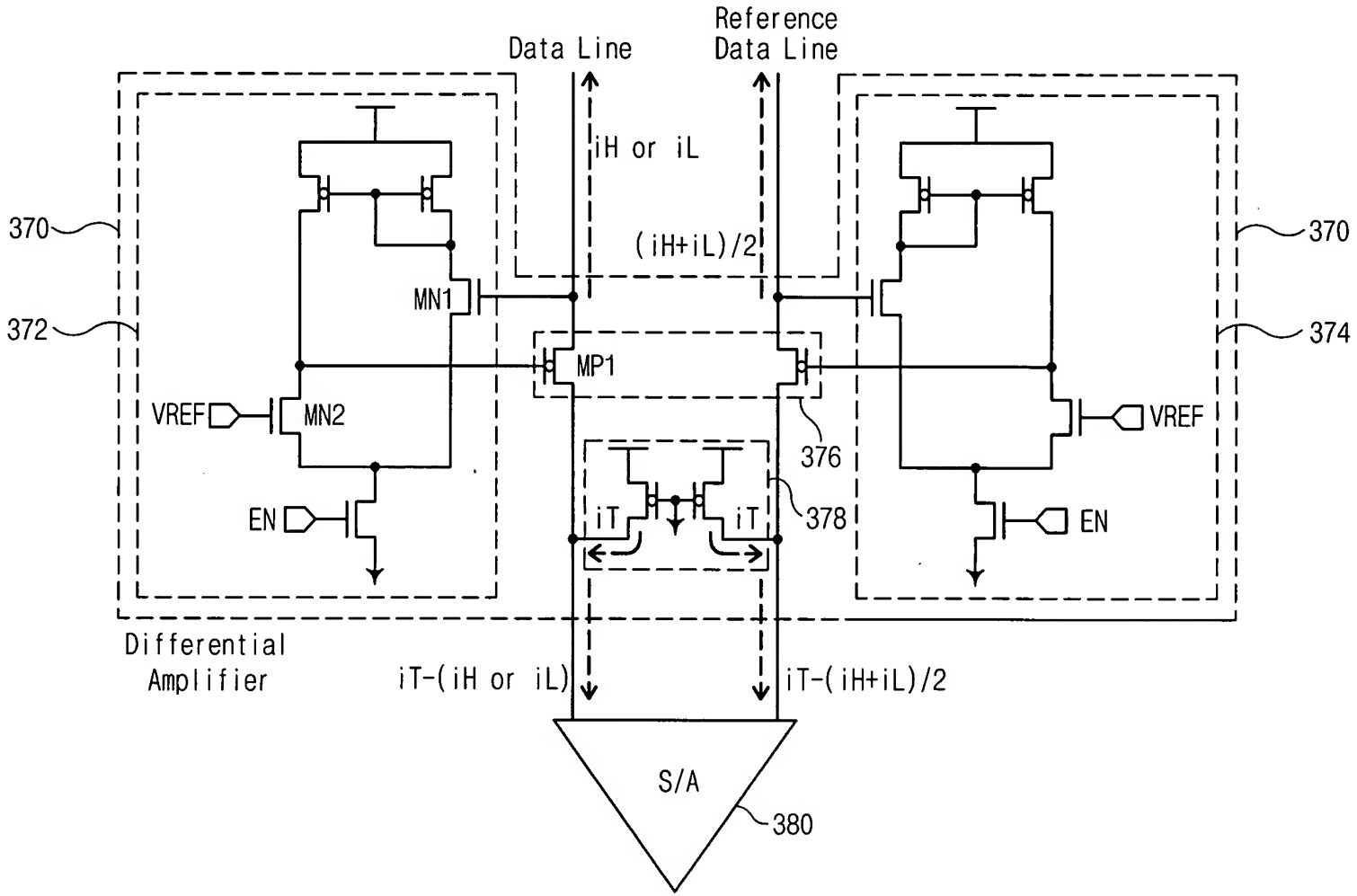
369
iH
iL
(iH+iL)/2
RBL0
RBL1
Reference BL

Fig. 5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Reference Data Line
iH or iL
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372
374
MN1
MP1
VREF
MN2
EN
376
iT
iT
378
Differential Amplifier
iT-(iH or iL)
iT-(iH+iL)/2
S/A
380